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Investigation and Implementation of Backup Supply Power Lines

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Abstract

This thesis aims to determine the most suitable topology by comparing the advantages of input power redundancy architectures used in avionics units for military aircraft (HA). Redundancy architectures for input power of avionics units were investigated, analyzed using LTSpice and the PCB design was optimized according to the analysis results. Then, based on the experimental and simulation results, the most suitable redundancy architectures were determined according to the criticality levels of avionics units and model validation studies were conducted. Both passive (e.g., resistors and diodes) and active redundancy structures (e.g., Switching Mode Power Supplies (SMPS), Low Dropout Regulators (LDOs) and MOSFETs) were investigated. Integrated components were selected for circuit design and analysis by complying with the standard test procedures outlined in MIL-STD-810, MIL-STD-461 and MIL-STD-704. Circuit diagrams were designed using LTSpice and Ansys SIWave Simulation software and thermal, direct current (DC) and frequency analyses were performed. Efficiency and output voltage fluctuations were evaluated to compare different redundancy architectures. The layout design was optimized using Altium software, which included current and power density evaluations. After the PCB (Printed Circuit Board) design was completed, production documentation was prepared, manufacturers were contacted and PCBs were manufactured. The manufactured PCBs went through typesetting and quality control procedures. A special test setup was created for the initial power test and a test procedure was developed to perform functionality, thermal and power tests using appropriate test equipment including oscilloscopes, multimeters, environmental test chambers and load banks. Environmental-mental tests were conducted in accordance with MIL-STD-810 standards to simulate operating conditions at varying altitudes and temperatures, including thermal shock, cold start performance, minimum-maximum operating conditions and long-term operational stability evaluations.

Subject Areas

Electric Engineering

Keywords

Power Redundancy, Current Sharing, Parallel Operation,
MIL-STD Compliance, Circuit Simulation

1. Introduction

Today's high-power applications, particularly in industrial, military, and commercial systems, demand efficient power supply management and high reliability.

The increasing complexity of electronic devices, the need for higher microprocessor computational speeds, and the growing focus on environmentally friendly electronics have introduced stringent requirements for power supplies [1]. To enhance power supply efficiency and reduce factors affecting system reliability—such as conduction losses, switching losses, and thermal losses—improvements in the power stage of the design are essential. Furthermore, power system topologies have evolved to meet the high power demands of emerging technologies, while also ensuring system performance and efficiency within the same physical dimensions. In this context, load sharing among multiple DC-DC converters operating in parallel has become a critical feature to enhance overall system efficiency and provide redundancy in overload situations.

Current sharing refers to a method in which each converter carries an equal portion of the load by distributing the output currents of multiple converters in a balanced manner [2]. Poorly designed current-sharing mechanisms can result in excessive load current being drawn by one or more modules, leading to increased thermal stress and reduced system reliability [3]. Several current-sharing methods with varying complexities and performance characteristics have been proposed over time [3]. Among these, the simplest and most cost-effective method is the voltage drop technique.

In the voltage drop method, the outputs of the power supplies are either directly connected or shared through a series resistor. As the load current increases, the output voltage of the power supply decreases [3].

However, with advancing technology, the current-sharing method has emerged as an improvement over the voltage drop method. The current-sharing technique aims to balance the load across all converters, and it primarily utilizes passive components (such as resistors) and active components (such as SMPS, LDOs, MOSFETs, diodes, etc.). A control mechanism is also employed to equalize the currents drawn from the redundant power modules, utilizing voltage and current feedback loops.

This document explores redundant power supply architectures, their practical applications, the operation of current-sharing functions, optimization strategies for these functions, and methods to ensure redundancy in power systems.

2. Method

After the widespread use of electricity, engineers developed various methods to convert electrical power into different forms and adjust it to different voltage levels. Linear power supplies are among the oldest methods of voltage conversion.

The system algebra method is used to verify the system design against requirements, validate its functionality over time, and assess fault tolerance by examining the system's state transitions under component or subsystem failures [4]. A comparison of the Fault Containment Subsystems (FCS) of the Airbus A380 and Boeing 777 demonstrates the capability of system algebra to evaluate the critical features of similar systems [4]. While system algebra highlights the dependencies of system security on subcomponents, it also defines the requirements for subsystems and their components.

Determining the appropriate power redundancy method is one of the primary security measures in system architecture. The degree of input power redundancy and the chosen methodology depend on the specific application of the system. For instance, the power redundancy requirements for flight-critical avionics, such as the Flight Computer and Inertial Measurement Unit (IMU), differ significantly from those for non-flight-critical environmental sensors. The power values (current, voltage) applied to the system determine the protection elements required at the system input.

When designing the power redundancy architecture, the avionics affected in the event of a potential failure, along with the risk analyses of these avionics within the general system architecture, help define the system's power supply lines and the interface components that must be connected to these lines.

In this section of the paper, power system redundancy methods, the disadvantages of these methods during the design phase, and possible solutions to address these disadvantages will be explained in sequence. Finally, optimization strategies aimed at enhancing system security will be discussed.

2.1. Power Redundancy with Resistance

Power redundancy using resistance is one of the most commonly employed and straightforward methods by designers in system architecture. In this method, the outputs of power supplies are shared through resistors, and during PCB material placement and routing (Placement-Routing), the line resistance can be taken into account and shared accordingly. Although this method may appear attractive due to its low cost and ease of schematic (SCH) and PCB design, it has several significant disadvantages.

Advantages:

- Easy to use and design.
- Cost-effective.

Disadvantages:

- There is a risk of systems feeding each other, as reverse voltage protection is not implemented.

- Current sharing cannot be performed equally due to the tolerance of the resistors used for backup and the impedance of the PCB lines.
- If any redundant power supply fails, the entire system power is lost. Therefore, full power redundancy cannot be achieved.
- Heat accumulates in the system based on the resistance value used for power supply sharing, which reduces system reliability.
- The system power cannot be turned on or off in a controlled manner.
- The layout challenges that arise in current sharing due to the impedance of PCB lines during the design phase.

For example, in the case of an LDO providing two 3.3V outputs, where the output voltage tolerance is 3%, the common resistance is 2 Ohms, and the current requested from the output is calculated as 1A (ignoring the PCB line impedance) [5]:

Worst-case scenario:

- LDO1 output: $3.3 \cdot 103100 = 3.4V$
- LDO2 output: $3.3 \cdot 97100 = 3.2V$

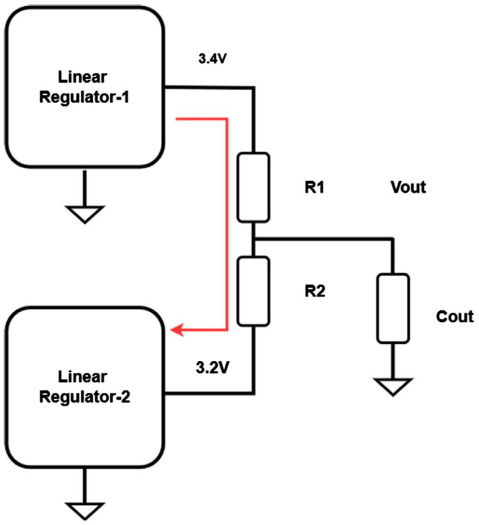

Figure 1. Redundancy with Resistance.

As shown in **Figure 1** [5], there will be a current flow demand from LDO1 to LDO2. Furthermore, since resistance is used as a backup method, a short-circuit fault occurring at the output of either LDO1 or LDO2 would result in a power failure throughout the entire system.

Passive redundancy can be achieved without using physical resistive elements by modeling the line impedances and parasitic impedances in the PCB layout design. While, in theory, line impedances can be equalized, this is not feasible in practice. According to IPC standards, the thickness of the conductive layers used in the manufacturing process and the insulators between them have certain tolerances. Due to these tolerances, it is impossible to achieve perfectly equal impedance in real-world applications.

2.2. Redundancy with Diode

Schottky diodes are commonly used to enhance system redundancy or increase power capacity in an N + 1 configuration (Figure 2). This method is traditionally employed to operate two or more power supplies in parallel. In an N + 1 redundant configuration, multiple power supply units (PSUs) are connected in parallel, with Schottky diodes facilitating the power distribution [6].

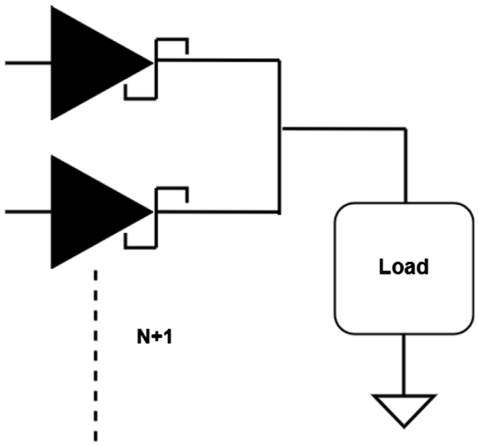

Figure 2. N + 1 Schottky Parallel Connection [6].

The Schottky diode semiconductor element is employed to overcome the disadvantages of the power backup method using resistance and to create a more reliable system. Since current can flow in only one direction through the diode, it provides reverse voltage protection. This functionality enhances the safety of the power backup, particularly in fault scenarios created by resistive elements in the redundancy architecture (Figure 3).

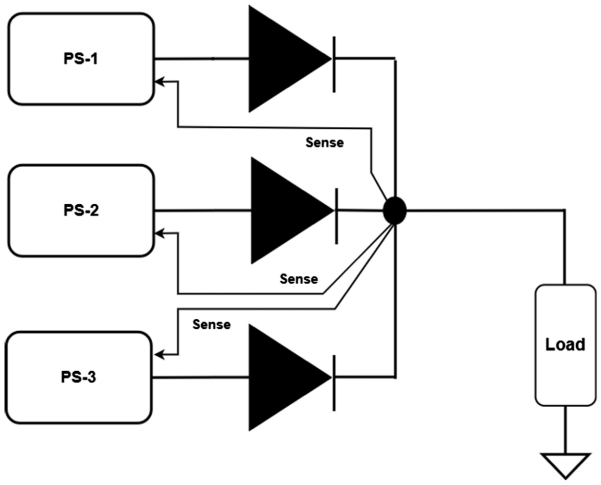

Figure 3. Diode Power Redundancy Architecture [7] [8].

In Figure 4, a linear voltage ranging from +12 V to −12 V is applied to the input of the D1 Schottky diode. When the input voltage drops below 0 V (*i.e.*, reverse

voltage is applied), the output voltage becomes 0 V, as shown in the graph.

Disadvantages of Using Diodes in Terms of System Security:

- **Forward Voltage Drop**: Variations in the forward voltage drop due to manufacturing tolerances of the diodes.
- **Lack of Controlled Power On/Off:** The system power cannot be turned on or off in a controlled manner.
- **Voltage Differences Due to Doping Variations:** Differences in voltage drops caused by variations in semiconductor doping during the production process.
- **Layout Challenges:** Difficulty in current sharing due to PCB line impedance during the design phase.

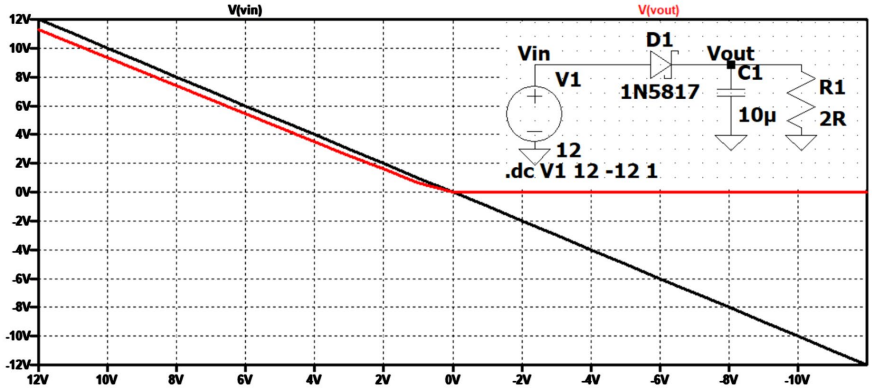

Figure 4. Reverse voltage protection.

Figure 5 illustrates the diode-based power backup architecture.

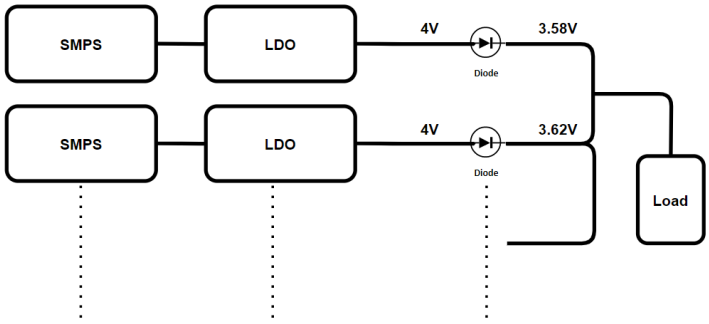

Figure 5. Diode power backup architecture.

When implementing power backup due to the forward voltage drop from the manufacturing process, the power outputs should be adjusted accordingly. In Figure 5, these voltage drops are considered to be 0.7 V in the ideal case. However, these values vary depending on the semiconductor doping material and the degree of doping. Additionally, not all products from a production line exhibit the same quality, nor do they have the same voltage drop characteristics.

For instance, when examining the electrical characteristics of the **SBR10U45SP5-13** Schottky diode, as shown in Figure 6 [9], it is observed that the forward voltage

varies depending on the current flowing through it and the temperature.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 7)	$V_{(BR)R}$	45	—	—	V	I_R = 0.3mA
Forward Voltage Drop	V_F	— — —	— 0.42 0.38	0.42 0.47 0.41	V	I_F = 8A, T_J = +25°C I_F = 10A, T_J = +25°C I_F = 10A, T_J = +125°C
Leakage Current (Note 7)	I_R	— — —	0.05 — 28.0	0.3 15 75	mA	V_R = 45V, T_J = +25°C V_R = 45V, T_J = +100°C V_R = 45V, T_J = +150°C

Figure 6. SBR10U45SP5-13 schottky diode electrical characteristic values.

When Figure 7 is examined, it can be observed that due to temperature variations caused by the placement of components on the PCB layout or differences in doping ratios during the manufacturing process, the voltage drop across **Diode1** is 0.42 V, while the voltage drop across **Diode2** is 0.38 V. These variations highlight the impact of both physical positioning and material properties on the diode's performance.

As shown in Figure 7, since the voltage on the **Diode2** power line is at a higher potential, the system demands current through the **Diode2** line, causing it to heat up more. As the diode heats up, its forward voltage drop decreases, placing additional strain on the diode. This can ultimately lead to damage to the diode.

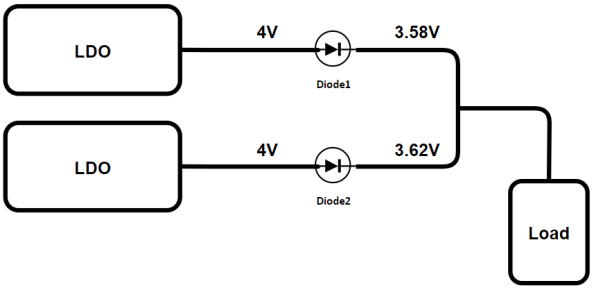

Figure 7. Power backup with diode with different forward voltage drop.

Two possible scenarios can arise from this condition:

- The diode may fall into a short circuit.
- The diode may fall into an open circuit.

When a high current flows through the diodes, the forward voltage decreases due to the temperature increase. Eventually, the junction between the diode's internal layers breaks down, causing the diode to open circuit.

In this case, the system will demand current from **Diode1**. If the diodes are not selected with the appropriate electrical characteristics to support the system independently, the same failure scenario that occurs with **Diode2** can also happen with **Diode1**, leading to a complete power failure in the system.

2.3. Power Redundancy with Oring Diode

The **Oring Diode** method is used to mitigate the effects of the forward voltage

drop in diodes and to enable controlled power switching on and off. This method enhances system reliability by incorporating an external MOSFET driver and additional peripheral components. However, it also introduces extra design complexity in the PCB layout and increases the overall system cost.

To simulate a diode using MOSFETs, two MOSFETs are required. The M1 MOSFET provides reverse voltage protection, while the M2 MOSFET handles the switching of the power line, as shown in Figure 8 [10].

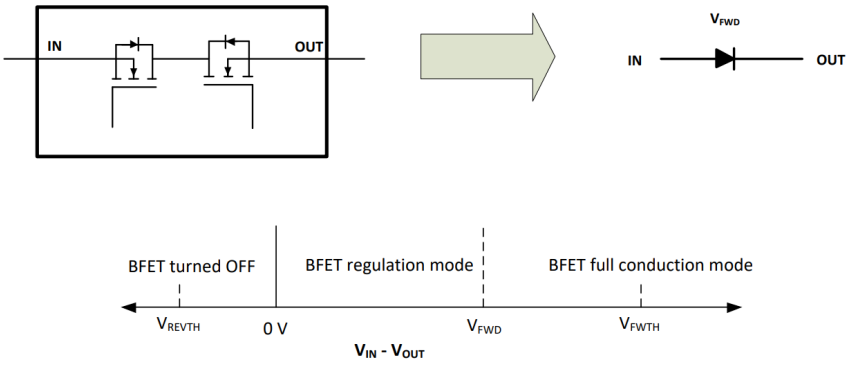

Figure 8. Implementation of Diode with Mosfets.

When the MOSFET is turned on, it introduces a resistance at the milliohm (mΩ) level due to its R_ds characteristic. As the system draws current, a voltage drop occurs across this resistance, resulting in an output voltage difference that is proportional to the resistance value. This voltage drop impacts the overall efficiency of the power system, particularly at higher current levels, since the resistance of the MOSFET contributes to power losses. An example of the power handling capability using MOSFETs in an Oring diode topology is illustrated in Figure 9.

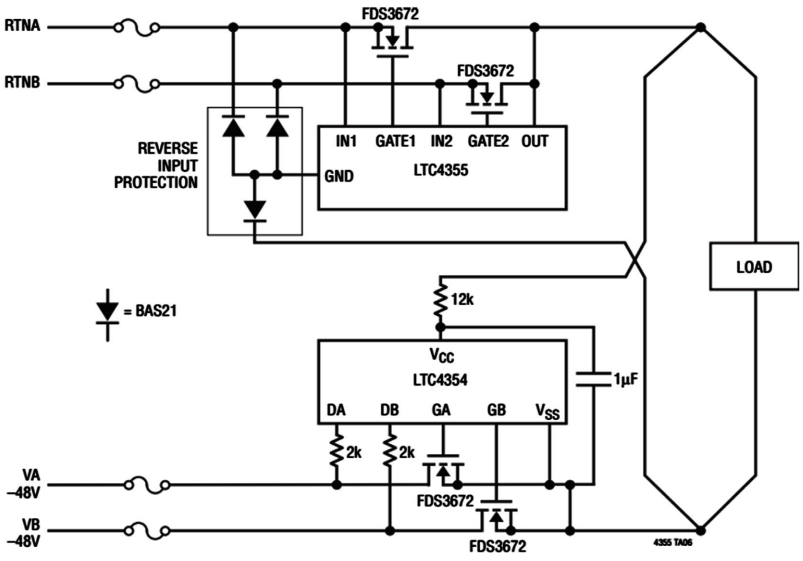

Figure 9. ORing Diode-Based Redundant Power Supply Schematic [11].

If the input voltage is 3.3 V, the load current is 1A, and the R_ds value of the MOSFET is taken as shown in Figure 10, the voltage drop across the MOSFET can be calculated as follows:

$$V_{drop} = R_{DS(on)} \cdot I_{load} = 6.7\ \text{m}\Omega \cdot 2 \cdot 1\ \text{A} = 13.4\ \text{mV} \quad (1)$$

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	7.8	12.1	mΩ
		V_{GS}=10 V, I_D=20 A	-	5.3	6.7	

Figure 10. BSZ067N06LS3 G electrical characteristic values [12].

Even in the ideal case, **Schottky diodes** exhibit a voltage drop of at least **300 mV**, which is significantly higher than the voltage drop across MOSFETs.

With advancements in semiconductor manufacturing, **newer fabrication processes** with lower nanometer technology enable the integration of **external MOSFET elements** into a single package within the **MOSFET driver structure,** as shown in Figure 11 [10]. This approach **optimizes PCB layout by saving space** and achieves a **lower Drain-Source resistance** compared to discrete MOSFET implementations. However, this integration **limits the designer's flexibility**, as the ability to customize and optimize the circuit based on specific design requirements is reduced.

Despite their higher cost and larger PCB footprint, O-ring diodes are increasingly adopted due to their ability to enhance system security. They are particularly prevalent in military applications and electric vehicle electronics, where reliability and redundancy are critical.

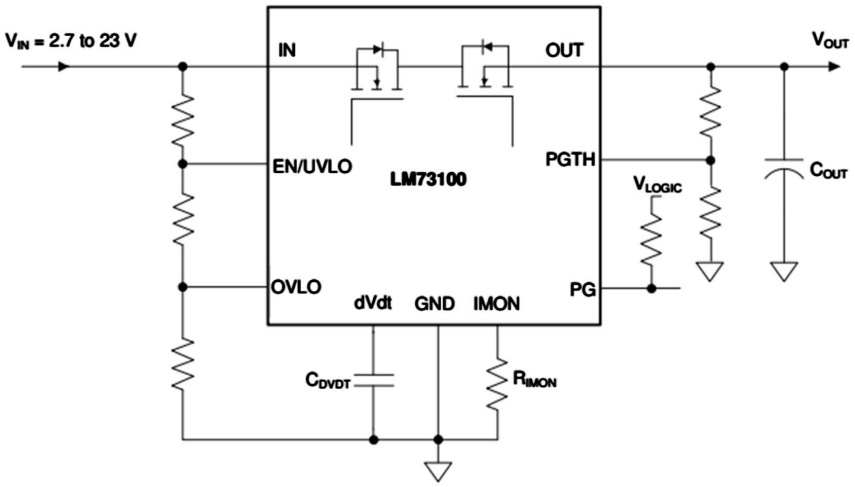

Figure 11. Fabricated example of the LM73100 MOSFETs and controller wire package.

2.4. Power Redundancy with Current Sharing and Parallel Connection

Although the current-sharing method using an O-ring diode serves as an alternative to the disadvantages of diode and resistance-based methods, it is not commonly preferred by module designers due to its increased system cost and larger

PCB footprint.

The increasing functional complexity of electronic devices, higher microprocessor computational speeds, and the growing demand for environmentally friendly electronics have imposed stringent requirements on power supply systems [1]. To enhance power supply efficiency and minimize reliability-affecting factors such as conduction loss, switching loss, and thermal loss, the power layer and associated loads must be placed in close proximity to the PCB layout. Furthermore, modular designs face a growing need to convert high power levels within limited board space while efficiently transmitting high load currents (>4 A).

Advancements in technology have enabled the parallel connection of voltage converters such as SMPS and LDO to meet these requirements. These converters regulate their output voltage using either Voltage Mode Control (VMC) or Current Mode Control (CMC), with the necessary current and voltage feedback provided according to manufacturer specifications.

VMC offers several advantages over CMC. In CMC, high di/dt cycle-to-cycle current information is injected into the feedback loop to generate a ramp voltage, which is then fed into a Pulse-Width Modulation (PWM) comparator and compared to the error voltage. In contrast, VMC generates its ramp internally, making it less susceptible to noise and duty cycle jitter [13].

Figure 12 [14] illustrates the parallel connection of the LTM8064 SMPS integrated circuit with different input voltages and a fixed output voltage. According to the manufacturer's datasheet, the common pins (SS, SYNC, and IOUTMON) in the parallel connection are linked to the "Current Mode Controller" in the internal structure of the SMPS. The IOUTMON pin enables external adjustment of the SMPS by measuring its output current [14]. This feature allows the SMPS to transition from Constant Voltage (CV) mode to Constant Current (CC) mode in the event of a short circuit at the outputs, thereby reducing the output voltage [14].

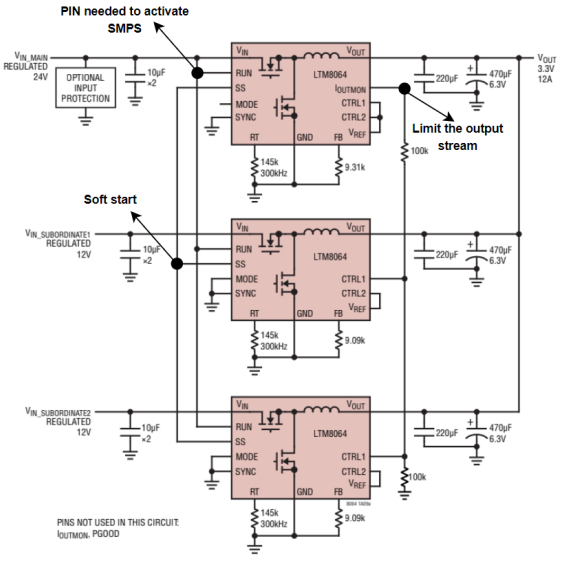

Figure 12. LTM8064 SMPS parallel connection [14].

Figure 12 [14] and Figure 13 [15] illustrate the parallel circuit topologies of the LTM8064 and LT3083 integrated circuits, respectively. According to the manufacturer's datasheet, the common pins used in parallel connection—SS, SYNC, and I_{OUTMON} are internally connected to the "Current Mode Controller" within the SMPS structure. The I_{OUTMON} pin enables external regulation of the SMPS by monitoring the output current [14]. This feature allows the SMPS to transition from Constant Voltage (CV) to Constant Current (CC) mode in the event of a short circuit at the output, thereby reducing the output voltage [14].

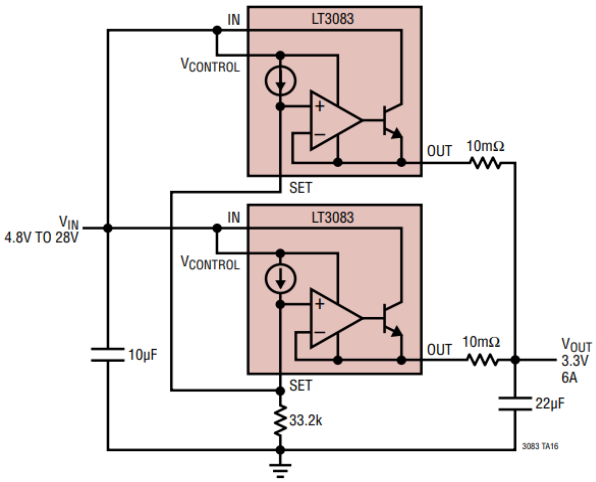

Figure 13. LT3083 LDO Parallel Connection [15].

2.5. Optimization Studies

Both passive and active power redundancy have their respective advantages. The designer should leverage these advantages when making improvements in the system design.

Power and communication redundancy should be integrated into the overall system architecture. For example, if two avionics units perform the same task in a High Availability (HA) system, the power for these units should be supplied from different sources. They should communicate with other avionics units using at least two different communication protocols, and these communication buses should be independent of each other. This ensures a two-redundant architecture is established for each unit without redundancy loss. To increase system reliability, the system architecture, the criticality level of the avionics, and the weakest points in the system's failure response must be well-understood by the designer.

Key Steps for Power Redundancy Design:

- **Power and Communication Architecture:** Define the power and **communication** structures based on the system requirements.
- **Criticality Level of Avionics: Determine** the criticality level of each avionics unit in the architecture to understand the system's vulnerability.
- **Power Redundancy Structure:** Based on the criticality level, select an appropriate power redundancy method to ensure system security.

These three stages will guide the selection of the appropriate power redundancy method.

System Optimization After Implementing Redundancy

Once redundancy is established, the following steps ensure system optimization:

- **Material Selection:** Choose materials based on operating voltage and current requirements while considering environmental factors such as temperature, voltage fluctuations, current variations, and Electromagnetic Interference (EMI) resistance. For military applications, materials should comply with standards such as MIL-STD 810, MIL-STD 704, and MIL-STD 461.
- **Input Protection Mechanisms:** Implement protective components such as TVS (Transient Voltage Suppressors), fuses, surge stoppers, CMC (Common Mode Coils), and passive LC filters to safeguard inputs.
- **Output Current Protection:** Integrate output current protection based on load current specifications.
- **Short Circuit and Thermal Protection:** Design output short circuit and thermal protection mechanisms to prevent damage during faults [16].
- **Voltage Protection:** Implement Under Voltage (UV) and Over Voltage (OV) protection to maintain a stable operational input voltage range.
- **Simulation and Circuit Modeling:** Evaluate protection structures using simulation tools like LTSpice to verify performance before implementation.
- **Schematic (SCH) and PCB Design:** Develop verified circuit topologies using Altium Designer or equivalent design software.
- **PCB Optimization:** Perform current density, power density, thermal analysis, frequency analysis, and DC analysis using simulation tools such as Altium or Ansys SIWave to refine PCB design before production.

INTEGRATED SELECTION

The first stage of the design process involves selecting appropriate materials based on the specific requirements and intended application of the avionics system. The parameters considered during material selection are presented in **Table 1**.

Table 1. Design requirements for current sharing and parallel operation designs.

Parameter	Requirement	Description
Input Voltage (V_{in})	≤50 V	Input voltage operating range
Output Voltage (V_{out})	1.2 V ≤ V_{out} ≤ 26 V	Output voltage operating range
Output Current (I_{out})	≥3 A	Minimum output current level
Operating Temperature (T_{op})	≥105˚C	Minimum operational working temperature
Output Current Monitoring (I_{outmon})	1 A	Output current monitoring level
Soft Start (T_{rss})	≥15 ms	Soft start time

To utilize the main input voltage in the design, the SMPS from Analog Devices, model **LTM8064IY#PBF**, was selected. The operational temperature range of LTM8064IY#PBF is −40˚C to 125˚C.

The calculated values are based on the reference data from Figure 12.

$$R_{fb} = \frac{19.44}{V_{out} - 1.2} \tag{2}$$

where R_{fb} is in kΩ.

A feedback *resistor* of $R_{fb} = 5.11\ \text{k}\Omega$ is used for $V_{out} = 5\ \text{V}$.

The operational input voltage range of LTM8064IY#PBF is $6\ \text{V} \le V_{in} \le 58\ \text{V}$.

$$R_1 = \frac{1.52 \cdot R_2}{UVLO - 1.52} \tag{3}$$

In the system, the *RUN* pin of the LTM8064IY#PBF integrated circuit is directly connected to the input voltage, enabling the system to power up.

$$I_{\text{outmax}} = \frac{9.31 \cdot R_2}{R_1 - R_2} \tag{4}$$

By selecting R_2 = 1 kΩ and R_1 = 8.3 kΩ, the *output* current limit is set to 1 A.

$$t_{ss} = \frac{C_{ss} \cdot V_{ref}}{I_{ss}} \tag{5}$$

A capacitance of $C_{ss} = 100\ \text{nF}$ was selected, setting the Soft-Start time to 18 ms.

$$T_J = T_A + \left(P_{loss} \cdot Q_{JA}\right) \tag{6}$$

For $T_J = 125^{\circ}\text{C}$, $Q_{JA} = 13.8^{\circ}\text{C/W}$ and $T_A = 85^{\circ}\text{C}$ values of the LTM8064IY#PBF integrated circuit;

$$P_{loss} = \frac{125^{\circ}\text{C} - 85^{\circ}\text{C}}{13.8^{\circ}\text{C/W}} = 2.89\ \text{W} \tag{7}$$

The loss that will occur due to the efficiency of the SMPS, based on V_{in} = 36 V and V_{out} = 5 V/3 A output, is calculated as follows:

$$P = V_{out} \cdot I_{out} \tag{8}$$

$$P_{loss} = V_{out} \cdot I_{out} \cdot \%loss \tag{9}$$

$$P_{loss} = 5\ \text{V} \cdot 3\ \text{A} \cdot 0.15 = 2.25\ \text{W} \tag{10}$$

The operational temperature range of the LT3083 is −40˚C to 125˚C.

$$V_{out} = 50\ \text{uA} \cdot R_{set} \tag{11}$$

Therefore, the SMPS output voltage was set to 3.75 V by adding 3.3 V plus the Low Dropout Voltage (310 mV).

$$P_{OUT} = \left(3.75\ \text{V} - 3.3\ \text{V}\right) \cdot 3\ \text{A} = 1.35 \tag{12}$$

$$P_{TOTAL} = 1.35\ \text{W} + 16.5\ \text{mW} = 1.366\ \text{W} \tag{13}$$

$$T_J = 50^{\circ}\text{C} + 1.366\ \text{W} \cdot 16^{\circ}\text{C/W} = 71^{\circ}\text{C} \tag{14}$$

After the SMPS, the Ideal Diode Control integrated circuit with the manufac-

turer code LTC4352HMS#PBF from Analog Devices was used in the cascade configuration. The operational temperature range of the LTC4352HMS#PBF is −40˚C to 150˚C.

$$P = I_{load}^2 \cdot R_{DS(ON)} = (3\text{ A})^2 \cdot 4\text{ m}\Omega = 36\text{ mW} \quad (15)$$

Military standards such as **MIL-STD 810**, **MIL-STD 461**, and **MIL-STD 704** impose specific limitations on material choices. These standards dictate the performance and reliability characteristics required for avionics systems used in military applications.

For example, Figure 14 [17] illustrates the **MIL-STD 704F LDC105 test procedure**. Both the **MIL-STD 704F LDC105** and **MIL-STD-704F LDC302** tests share similar test steps, test schemes, and voltage levels [17]. However, there is a key difference in the duration for which the voltage is applied: while the MIL-STD 704F LDC105 High Voltage Transient Application test applies 50 V for 12.5 milliseconds, the MIL-STD-704F LDC302 test applies the same 50 V for 50 milliseconds.

To pass these tests successfully, the protection components selected—such as **TVS** (Transient Voltage Suppressors) and **Surge Stoppers**—must be chosen carefully. They need to withstand the different stress levels imposed by both test conditions.

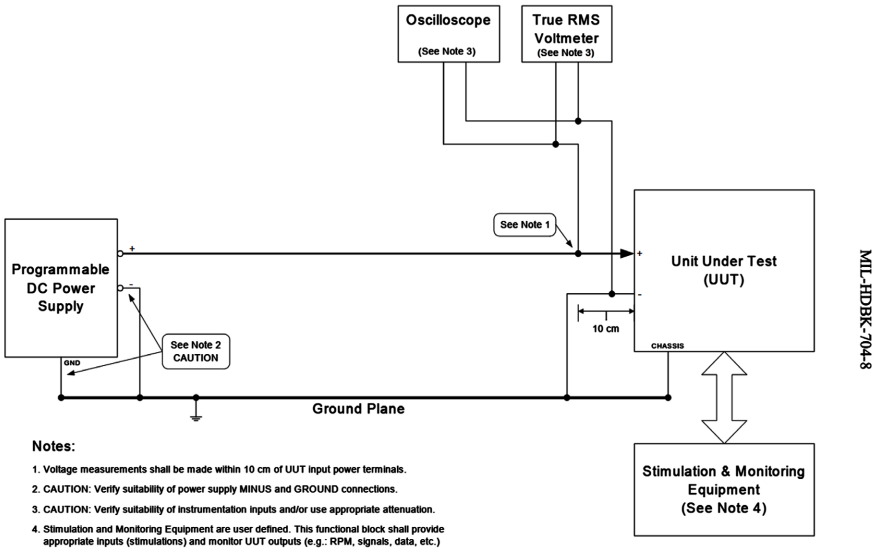

Figure 14. LDC105 Test MIL-HDBK-704-8 Reference Test Chart [17].

To meet the reverse voltage test requirements of the **MIL-STD 704F** standard, the reverse voltage protection was achieved by implementing a **"Back to Back" MOSFET** connection in the O-ring diode topology or by attaching a series **Schottky diode** to the output.

For all system elements to pass the **MIL-STD 810H** air conditioning tests, the operating temperature range was selected to operate between **−40˚C** and **+125˚C**.

An **EMI sealed box design** was created to pass the **MIL-STD 461** Radiated Emissions tests. Additionally, a **6A input filter design** was implemented to pass the **Conducted Emissions** tests.

3. Analysis And Design

During the design phase, analyses were performed using **LTSpice, Altium Designer, and Ansys SIwave** simulation tools. Each software played a critical role in addressing different aspects of the system's design and validation. LTSpice was used to simulate and verify circuit behavior under varying operating conditions, ensuring electrical functionality and stability. Altium Designer facilitated the creation of the PCB layout, enabling precise placement and routing of components according to design constraints. Ansys SIwave was utilized for signal integrity and electromagnetic compatibility (EMC) analysis, which is particularly important for avionics systems operating in sensitive environments.

The design was iteratively refined and optimized based on the simulation results. For example, adjustments were made to component values and layout geometries to reduce noise, improve power distribution, and enhance thermal performance.

The overall block diagram of the system is presented in Figure 15, providing a high-level view of the architectural and functional flow. Figure 19 shows the detailed circuit topologies used in the design, while Figure 20 shows the simulation test setup used to validate the operational scenarios. The LTSpice simulation results are shown in Figure 16 and Figure 17. These results validate the effectiveness of the selected components and design choices by verifying that the power supply operates properly under normal and transient conditions.

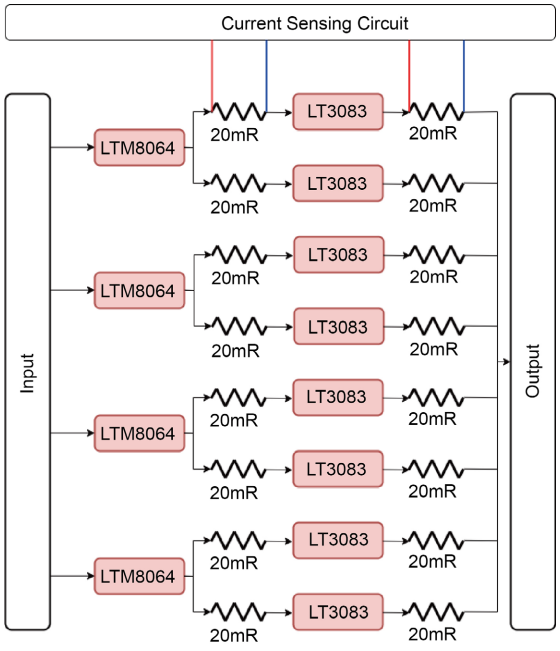

Figure 15. Block diagram of design.

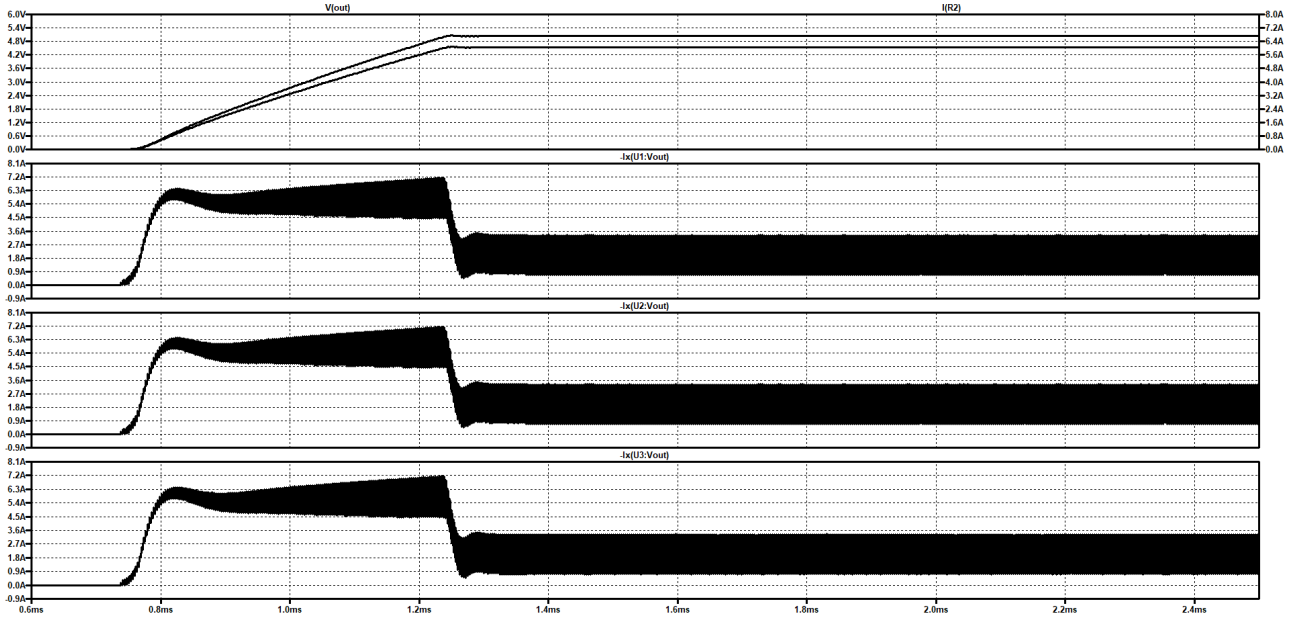

Figure 16. Output Ripple Analysis of the LTM8064 SMPS at 6A Load Current.

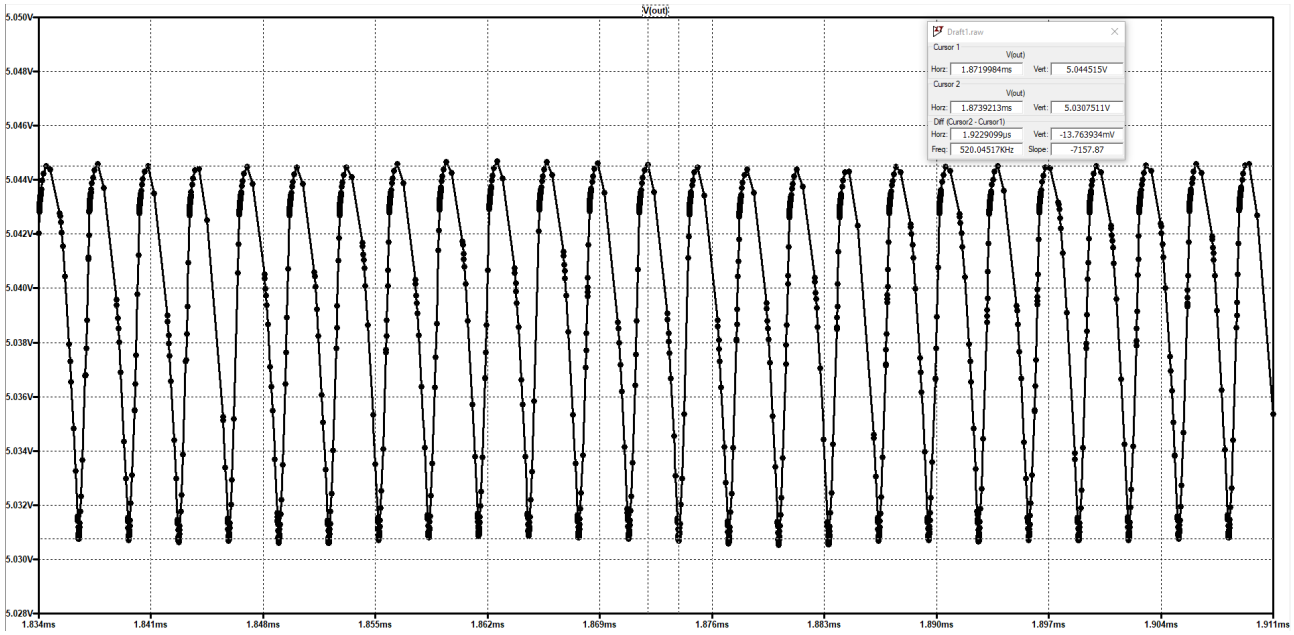

Figure 17. Output Ripple Analysis of the LTM8064 SMPS at 6A Load Current.

The schematic design of the selected LDO, SMPS and ORing Diode is presented in Figure 19. This figure shows the interconnections and basic components of the selected elements for power backup methods.

The design includes four spare power input ranges, each derived from one of the circuit blocks shown in Figure 19. Additionally, three different circuits were configured by adjusting the output voltages, redundancy topologies, and array types.

The **LTM8064** IC selected for the design offers an adjustable output current of

up to **7A**. As illustrated in the block diagram in Figure 18, the output of the **U2 IC (+VCC_Out3)** was optimized using **Altium Designer PDN (Power Distribution Network) analysis**. Subsequently, the PCB design was updated to enhance both performance and reliability (Figure 19 and Figure 20).

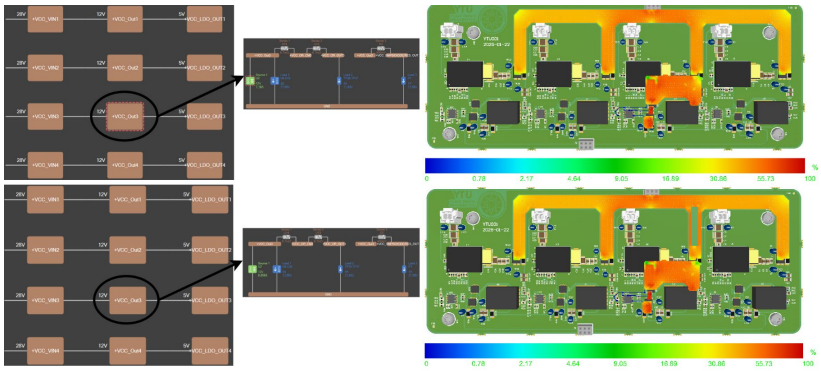

Figure 18. LTSpice Load Sharing Analysis of the LTM8064 SMPS under 6A Load.

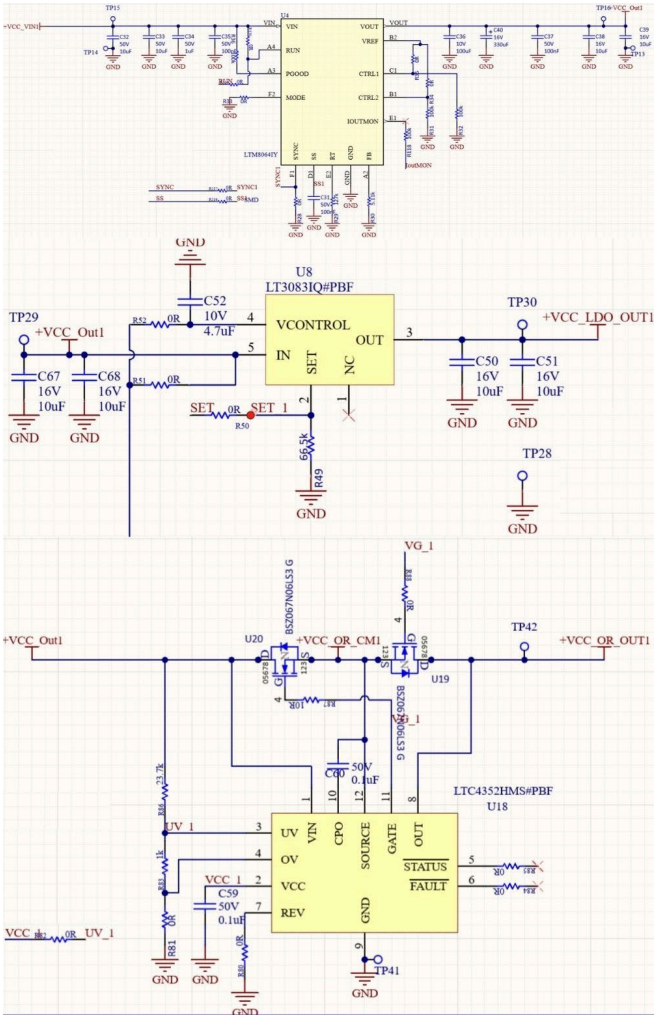

Figure 19. Schematic design of the selected LDO, SMPS, and ORing Diode.

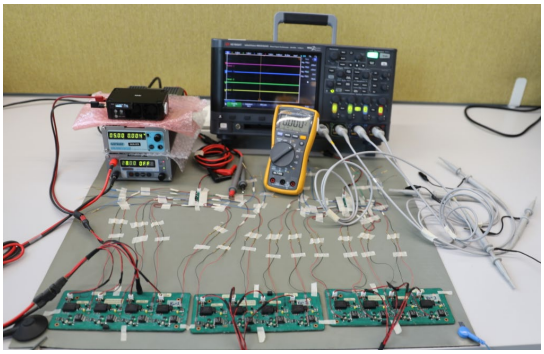

Figure 20. Functionality test setup showing measurement of load current, temperature and output voltage.

4. Test Process & Results

Three different circuit designs were implemented, and their performance tests were conducted.

$$V_{out} = I \cdot R_{Sense} \cdot Gain \tag{26}$$

Since the **LTSpice** simulation was performed under ideal conditions, it was observed that the current sharing between the **LTM8064** SMPS units was equal. However, in real-world applications, several non-ideal factors such as PCB trace impedance, semiconductor MOSFET manufacturing tolerances within the SMPS internal structure, and tolerances of external passive components must be taken into account. These factors lead to unbalanced current sharing between parallel power modules.

The desktop test results of the redundant power card, which was designed using a combination of SMPS, Oring Diodes, and LDOs, are summarized in Table 2. These results provide insight into the real-world performance and validate the redundancy strategy employed in the design.

Table 2. Output Current Distribution in SMPS, ORing Diode and LDO Topologies During Functionality Tests.

Topoloji	Akım Monitor Çıkışı	Kanal Akımı	Çıkı Yük Akımı
SMPS 1	1.616 V	1.616 V	6 A
SMPS 2	1.606 V	1.606 V	6 A
SMPS 3	1.824 V	1.824 V	6 A
SMPS 4	0.913 V	0.913 V	6 A
Oring 1	1.932 V	1.932 V	6 A
Oring 2	1.887 V	1.887 V	6 A
Oring 3	0.940 V	0.940 V	6 A
Oring 4	0.995 V	0.995 V	6 A
LDO 1	0.303 V	0.303 V	4 A
LDO2	0.647 V	0.647 V	4 A
LDO3	0.801 V	0.801 V	4 A
LDO 4	0.985 V	0.985 V	4 A

$$P_{DRIVE} = \left(V_{CONTROL} - V_{out}\right) \cdot I_{CONTROL} \tag{16}$$

$$P_{TOTAL} = P_{DRIVE} + P_{OUTPUT} \tag{17}$$

$$P_{DRIVE} = \left(3.630\ \text{V} - 3.3\ \text{V}\right) \cdot 50\ \text{mA} = 16.5\ \text{mW} \tag{18}$$

$$P_{OUT} = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \tag{19}$$

$$I_{CONTROL} = \frac{I_{OUT}}{60} \tag{20}$$

$$I_{OUT} = 4\ \text{A}; I_{CONTROL} = \frac{4\ \text{A}}{60} = 66.66\ \text{mA} \tag{21}$$

$$P_{OUT} = \left(5\ \text{V} - 3.3\ \text{V}\right) \cdot 4\ \text{A} = 6.8\ \text{W} \tag{22}$$

$$P_{TOTAL} = 6.8\ \text{W} + 16.5\ \text{mW} = 6.816\ \text{W} \tag{23}$$

$$T_J = T_A + P_{TOTAL} \cdot Q_{JA} \tag{24}$$

$$T_J = 25^{\circ}\text{C} + 6.816\ \text{W} \cdot 16^{\circ}\text{C/W} = 134^{\circ}\text{C} \tag{25}$$

During benchtop functionality tests, the LTM8064 SMPS reached a temperature of 60˚C under a 6 A load, while the LTC4352 ORing Diode measured 65.2˚C under the same load conditions. Additionally, the LT3083 LDO regulator reached 109˚C under a 4 A load. These thermal performance results are illustrated in Figure 21.

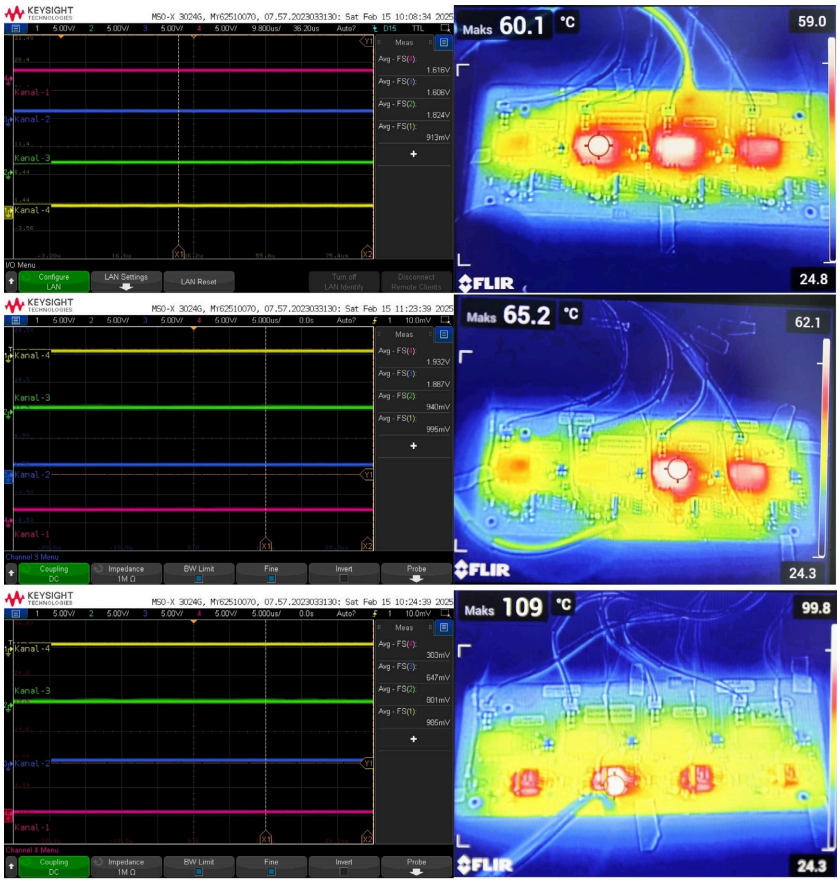

Figure 21. LTM8064 SMPS, LTC4352 ORing Diode, and LT3083 LDO Overload Test and Thermal Performance.

5. Conclusions

This study presents methods for implementing system redundancy at the power layer based on the operational environments of the units and evaluates their advantages and disadvantages. One of the most critical aspects of ensuring system redundancy in civil and unmanned aerial vehicles is power redundancy. If power redundancy is not properly implemented, failures in these systems can lead to severe risks, including aircraft crashes or structural damage.

The proposed redundancy topologies and their impact on system performance are analyzed in detail. The circuit design incorporating these topologies is illustrated in Figure 19. To enhance system reliability, optimization studies have been conducted, and the necessary formulations for material selection are provided. Depending on the selected power redundancy topology, system current can be evenly distributed among power converters, and power continuity can be ensured even if one or more converters fail. Additionally, the chosen topology can integrate various protection mechanisms, including reverse voltage protection, overvoltage protection, undervoltage protection, output short-circuit protection, and overcurrent protection, thereby enhancing system security.

The performance of different power redundancy topologies is evaluated through simulations, functionality tests, MIL-STD-810 environmental tests, and MIL-STD-704 compliance tests. Pre-design simulations help identify potential failures in advance, preventing issues during functionality tests. Moreover, optimizing the circuit size and selecting the most suitable topology contribute to improved system efficiency and reduced costs.

Conflicts of Interest

The authors declare no conflicts of interest.

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